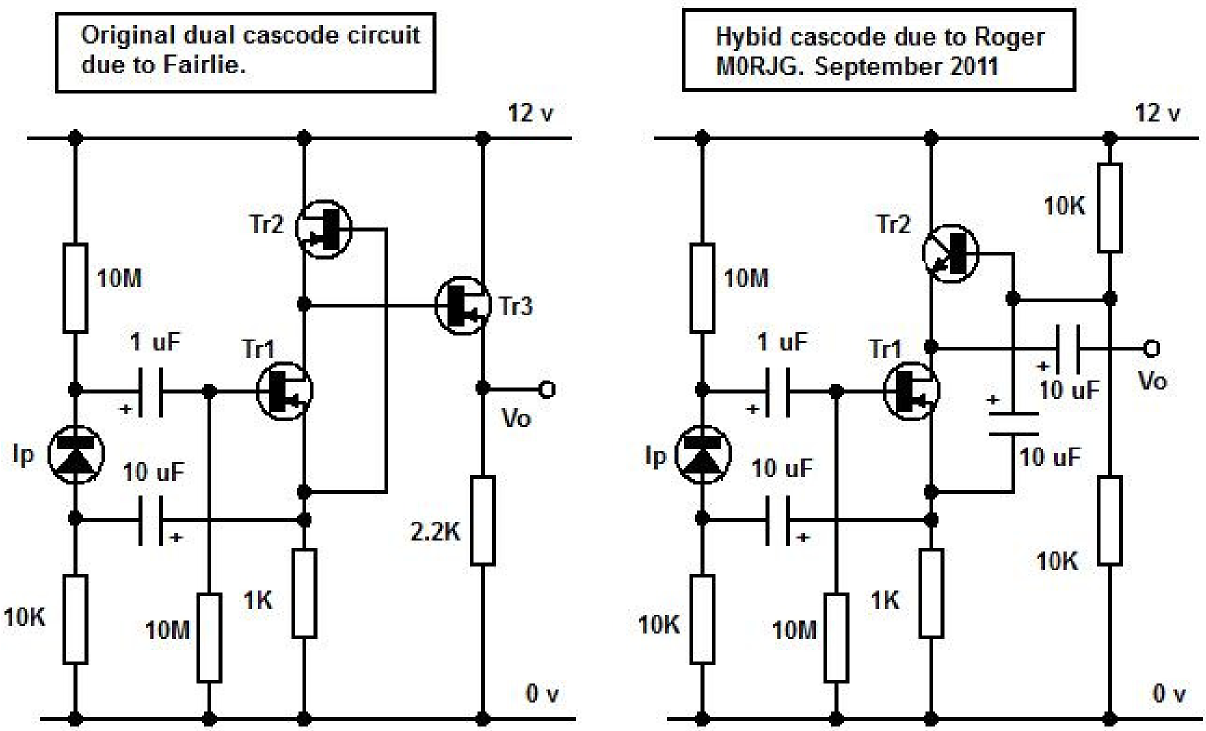
Cascode circuits – research outcomes, by Roger M0RJG.

Introduction.

The previous discussions concerned the merits of cascode circuits but all suffered from bandwidth limitations in the desire to obtain sensitivity, requiring equalisation further down the signal processing chain, and noise spectra were a problem under those conditions. The following circuits are reported which have the following advantages, being:

a) Improved bandwidth capabilities for a given photodiode, and
b) Vastly reduced Miller capacitance effects at the front end device.
c) No degradation of SNR over the bandwidth of interest, due to the fact that equalisation is no longer necessary.

There are two circuits presented, being one due to Fairlie (reference supplied on request), and a further development by the author.



Looking first at the Fairlie circuit on the left, the photodiode is conventionally connected to a 10M bias resistor acting as a load. At the other end is a 10K resistor which serves a different purpose. The output of the photodiode is firstly input to source follower Tr1. Its output then is fed back to the other side of the photodiode, and is almost the same amplitude as that from the top side of the photodiode as shown. The effect of photodiode capacitance is then reduced by a factor:

$Cd_{(eff)} = Cd.(1 - A)$, where A is the voltage gain of the source follower.

Note, if the amplifier were ideal, then the effective capacitance would be zero. Thus the bandwidth of the photodiode plus its load resistance is now:

$f_{3dB(eff)} = 1/[(2\pi.Cd.RL)(1 - A)]$, where RL is the load resistance, in this case set to 10M.

Therefore, much more signal can be obtained than previously, and before the (gain-bandwidth) product rule kicks in adversely, because the controlled positive feedback ensures that the bandwidth is enhanced in comparison to the uncorrected case, allowing a much higher value of RL to be used.

Next, the cascode circuit enhances something else. One of the issues with all the previous circuits is the Miller effect on the input stage due to feedback capacitance from the drain of Tr1 to its gate. In this case, there is a second feedback path in which the voltage at the source of Tr1 is then fed, via Tr2, to the drain of Tr1. Therefore, the gate-source has only a very small dV/dt component, meaning that the feedback capacitive current is also considerably reduced.

Thus the whole circuit has two bootstrapping circuits which serve to magnify the bandwidth capabilities of the first stage, allowing much larger load resistances RL to be used. The third transistor, Tr3, in the Fairlie circuit permits high impedance buffering to subsequent stages.

Turning attention to the M0RJG circuit, the second FET from the Fairlie circuit is replaced by a bipolar transistor which does the same job as Tr2 in the former circuit, with the added advantage of a direct low impedance output buffer to subsequent stages.

The positive feedback approach means that there is much more choice over circuit devices, as the effect is very strong and that specific, low capacitance devices are not so critically required. Note also that a larger photodiode may be used, which means more light can be collected, also improving sensitivity under marginal conditions (subject, of course, to the daylight overload aspects).

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